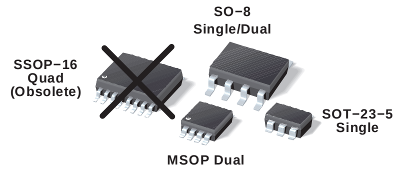
Burr-Brown Products from Texas Instruments



OPA237
OPA2237
OPA4237

SBOS057A − OCTOBER 1996 − REVISED FEBRUARY 2007

SINGLE-SUPPLY OPERATIONAL AMPLIFIERS
MicroAmplifier™ Series

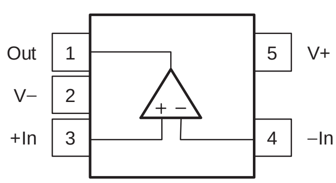
FEATURES

- **MICRO-SIZE, MINIATURE PACKAGES:**
  - **Single: SOT23-5, SO-8**
  - **Dual: MSOP-8, SO-8**
  - **Quad: SSOP-16 (Obsolete)**
- **LOW OFFSET VOLTAGE: 750μV max**
- **WIDE SUPPLY RANGE:**
  - **Single Supply: +2.7V to +36V**
  - **Dual Supply: ±1.35V to ±18V**
- **LOW QUIESCENT CURRENT: 350μV max**
- **WIDE BANDWIDTH: 1.5MHz**

APPLICATIONS

- **BATTERY-POWERED INSTRUMENTS**
- **PORTABLE DEVICES**
- **PCMCIA CARDS**
- **MEDICAL INSTRUMENTS**
- **TEST EQUIPMENT**

OPA237



SOT23−5

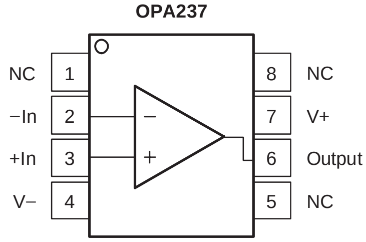
DESCRIPTION

The OPA237 op amp family is one of Texas Instruments' MicroAmplifier™ series of miniature products. In addition to small size, these devices feature low offset voltage, low quiescent current, low bias current, and a wide supply range. Single, dual, and quad versions have identical specifications for maximum design flexibility. They are ideal for single-supply, battery-operated, and space-limited applications, such as PCMCIA cards and other portable instruments.

OPA237 series op amps can operate from either single or dual supplies. When operated from a single supply, the input common-mode range extends below ground and the output can swing to within 10mV of ground. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction.

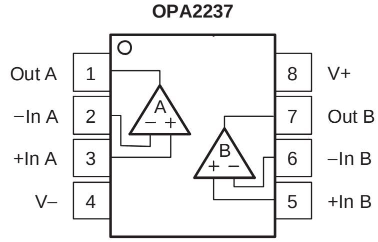
Single, dual, and quad are offered in space-saving surface-mount packages. The single version is available in the ultra-miniature 5-lead SOT23-5 and SO-8 surface-mount. The dual version comes in a miniature MSOP-8 and SO-8 surface-mount. The quad version is obsolete. MSOP-8 has the same lead count as a SO-8 but half the size. The SOT23-5 is even smaller at one-fourth the size of an SO-8. All are specified for −40°C to +85°C operation. A macromodel is available for design analysis.

OPA237



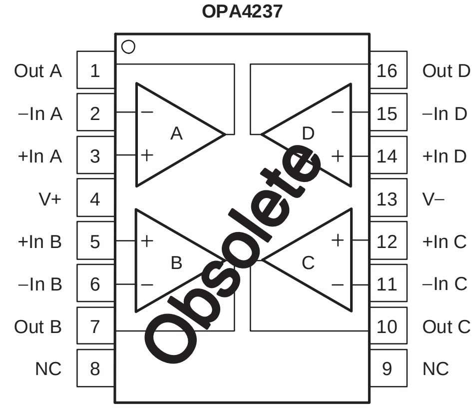
SO−8

OPA2237



SO−8, MSOP−8

OPA4237



SSOP−16

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ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage, V+ to V−	36V
Input Voltage	(V−) −0.7V to (V+) +0.7V
Output Short-Circuit(2)	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−55°C to +125°C
Junction Temperature Range	+150°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Short circuit to ground, one amplifier per package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE−LEAD	PACKAGE DRAWING	PACKAGE MARKING
Single OPA237NA	SOT23-5	DBV	A37A
OPA237UA	SO-8	D	OPA237UA
Dual OPA2237EA	MSOP-8	DGK	B37A
OPA2237UA	SO-8	D	OPA2237UA
Quad(2) OPA4237UA	SSOP-16	DBQ	OPA4237UA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Quad version is obsolete.

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits apply over the specified temperature range, **T_A = −40°C to +85°C**.

At T_A = +25°C, V_S = +5V, R_L = 10kΩ, connected to V_S/2, unless otherwise noted.

PARAMETER	CONDITIONS	OPA237UA, NA OPA2237UA, EA OPA4237UA MIN	TYP	MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage	V_{CM} = 2.5V		±250	±750	μV
vs Temperature(1)	**Specified Temperature Range**		**±2**	**±5**	**μV/°C**
vs Power Supply (PSRR)	V_S = +2.7V to +36V		10	30	μV/V
Channel Separation (dual and quad)			0.5		μV/V
INPUT BIAS CURRENT					
Input Bias Current(2)	V_{CM} = 2.5V		−10	−40	nA
Input Offset Current	V_{CM} = 2.5V		±0.5	±10	nA
NOISE					
Input Voltage Noise, f = 0.1 to 10Hz			1		μV_{PP}
Input Voltage Noise Density, f = 1kHz			28		$nV/\sqrt{Hz}$
Current Noise Density, f = 1kHz			60		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range		−0.2		(V+) −1.5	V
Common-Mode Rejection Ratio	V_{CM} = −0.2V to 3.5V	78	86		dB
INPUT IMPEDANCE					
Differential			$5 \bullet 10^6 \parallel 4$		Ω || pF
Common-Mode			$5 \bullet 10^9 \parallel 2$		Ω || pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = 0.5V to 4V	80	88		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product			1.4		MHz
Slew Rate	G = 1		0.5		V/μs
Settling Time, 0.1%	G = −1, 3V Step, C_L = 100pF		11		μs
0.01%	G = −1, 3V Step, C_L = 100pF		16		μs
OUTPUT					
Voltage Output, Positive	R_L = 100kΩ to Ground	(V+) −1	(V+) −0.75		V
Negative	R_L = 100kΩ to Ground	0.01	0.001		V
Positive	R_L = 100kΩ to 2.5V	(V+) −1	(V+) −0.75		V
Negative	R_L = 100kΩ to 2.5V	0.12	0.04		V
Positive	R_L = 10kΩ to 2.5V	(V+) −1	(V+) −0.75		V
Negative	R_L = 10kΩ to 2.5V	0.5	0.35		V
Short-Circuit Current			−10/+4		mA
Capacitive Load Drive (stable operation)		See Typical Characteristic Curves			
POWER SUPPLY					
Specified Operating Voltage			+5		V
Operating Range		+2.7		+36	V
Quiescent Current (per amplifier)			170	350	μA
TEMPERATURE RANGE					
Specified Range		−40		+85	°C
Operating Range		−55		+125	°C
Storage Range		−55		+125	°C
Thermal Resistance, θ_{JA}					
SOT23-5			200		°C/W
MSOP-8			150		°C/W
SSOP-16 (Obsolete)			150		°C/W
SO-8			150		°C/W

(1) Specified by wafer-level test to 95% confidence.
(2) Positive conventional current flows into the input terminals.

ELECTRICAL CHARACTERISTICS: V_S = +2.7V

Boldface limits apply over the specified temperature range, **T_A = −40°C to +85°C**.

At T_A = +25°C, V_S = +2.7V , R_L = 10kΩ, connected to V_S/2, unless otherwise noted.

PARAMETER	CONDITIONS	OPA237UA, NA OPA2237UA, EA OPA4237UA MIN	TYP	MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage	V_{CM} = 1V		±250	±750	µV
vs Temperature(1)	**Specified Temperature Range**		**±2**	**±5**	**µV/°C**
vs Power Supply (PSRR)	V_S = +2.7V to +36V		10	30	µV/V
Channel Separation (dual and quad)			0.5		µV/V
INPUT BIAS CURRENT					
Input Bias Current(2)	V_{CM} = 1V		−10	−40	nA
Input Offset Current	V_{CM} = 1V		±0.5	±10	nA
NOISE					
Input Voltage Noise, f = 0.1 to 10Hz			1		μV_{PP}
Input Voltage Noise Density, f = 1kHz			28		$nV/\sqrt{Hz}$
Current Noise Density, f = 1kHz			60		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range		−0.2		(V+) −1.5	V
Common-Mode Rejection Ratio	V_{CM} = −0.2V to 1.2V	75	85		dB
INPUT IMPEDANCE					
Differential			$5 \bullet 10^6 \parallel 4$		Ω || pF
Common-Mode			$5 \bullet 10^9 \parallel 2$		Ω || pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = 0.5V to 1.7V	80	88		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product			1.2		MHz
Slew Rate	G = 1		0.5		V/µs
Settling Time, 0.1%	G = −1, 1V Step, C_L = 100pF		5		µs
0.01%	G = −1, 1V Step, C_L = 100pF		8		µs
OUTPUT					
Voltage Output, Positive	R_L = 100kΩ to Ground	(V+) −1	(V+) −0.75		V
Negative	R_L = 100kΩ to Ground	0.01	0.001		V
Positive	R_L = 100kΩ to 1.35V	(V+) −1	(V+) −0.75		V
Negative	R_L = 100kΩ to 1.35V	0.06	0.02		V
Positive	R_L = 10kΩ to 1.35V	(V+) −1	(V+) −0.75		V
Negative	R_L = 10kΩ to 1.35V	0.3	0.2		V
Short-Circuit Current			−5/+3.5		mA
Capacitive Load Drive (stable operation)			See Typical Characteristic Curves		
POWER SUPPLY					
Specified Operating Voltage			+2.7		V
Operating Range		+2.7		+36	V
Quiescent Current (per amplifier)			160	350	µA
TEMPERATURE RANGE					
Specified Range		−40		+85	°C
Operating Range		−55		+125	°C
Storage Range		−55		+125	°C
Thermal Resistance, θ_{JA}					
SOT23-5			200		°C/W
MSOP-8			150		°C/W
SSOP-16 (Obsolete)			150		°C/W
SO-8			150		°C/W

(1) Specified by wafer-level test to 95% confidence.
(2) Positive conventional current flows into the input terminals.

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15V$

Boldface limits apply over the specified temperature range, **T_A = −40°C to +85°C**.

At T_A = +25°C, V_S = ±15V , R_L = 10kΩ, connected to V_S/2, unless otherwise noted.

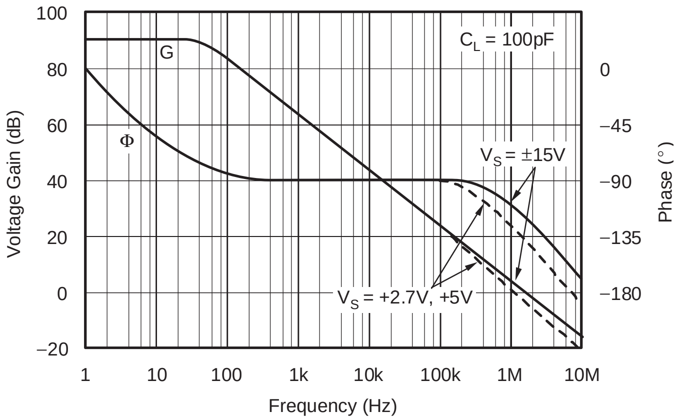
PARAMETER	CONDITIONS	OPA237UA, NA OPA2237UA, EA OPA4237UA MIN	TYP	MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage	V_{CM} = 0V		±350	±950	μV
vs Temperature(1)	**Specified Temperature Range**		**±2.5**	**±7**	**μV/°C**
vs Power Supply (PSRR)	V_S = ±1.35V to ±18V		10	30	μV/V
Channel Separation (dual and quad)			0.5		μV/V
INPUT BIAS CURRENT					
Input Bias Current(2)	V_{CM} = 0V		−8.5	−40	nA
Input Offset Current	V_{CM} = 0V		±0.5	±10	nA
NOISE					
Input Voltage Noise, f = 0.1 to 10Hz			1		μV_{PP}
Input Voltage Noise Density, f = 1kHz			28		$nV/\sqrt{Hz}$
Current Noise Density, f = 1kHz			60		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range		(V−)−0.2		(V+) −1.5	V
Common-Mode Rejection Ratio	V_{CM} = −15V to 13.5V	80	90		dB
INPUT IMPEDANCE					
Differential			$5 \bullet 10^6 \parallel 4$		Ω || pF
Common-Mode			$5 \bullet 10^9 \parallel 2$		Ω || pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = −14V to 13.8V	80	88		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product			1.5		MHz
Slew Rate	G = 1		0.5		V/μs
Settling Time, 0.1%	G = −1, 10V Step, C_L = 100pF		18		μs
0.01%	G = −1, 10V Step, C_L = 100pF		21		μs
OUTPUT					
Voltage Output, Positive	R_L = 100kΩ	(V+) −1.2	(V+) −0.9		V
Negative	R_L = 100kΩ	(V−) +0.5	(V−) +0.3		V
Positive	R_L = 10kΩ	(V+) −1.2	(V+) −0.9		V
Negative	R_L = 10kΩ	(V−) +1	(V−) +0.85		V
Short-Circuit Current			−8/+4.5		mA
Capacitive Load Drive (stable operation)		See Typical Characteristic Curves			
POWER SUPPLY					
Specified Operating Range			±15		V
Operating Range		±1.35		±18	V
Quiescent Current (per amplifier)			±200	±475	μA
TEMPERATURE RANGE					
Specified Range		−40		+85	°C
Operating Range		−55		+125	°C
Storage Range		−55		+125	°C
Thermal Resistance, θ_{JA}					
SOT23-5			200		°C/W
MSOP-8			150		°C/W
SSOP-16 (Obsolete)			150		°C/W
SO-8			150		°C/W

(1) Specified by wafer-level test to 95% confidence.
(2) Positive conventional current flows into the input terminals.

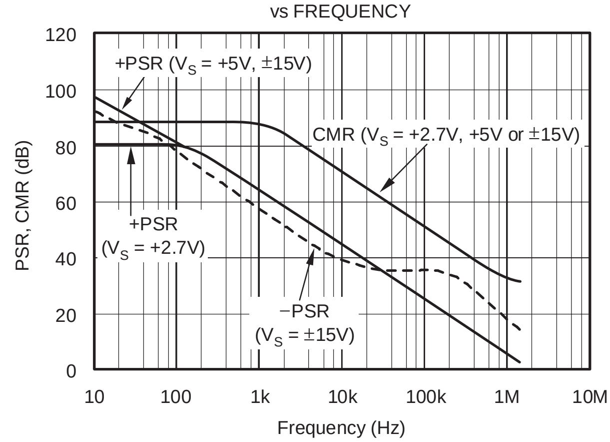
TYPICAL CHARACTERISTICS

At T_A = +25°C and R_L = 10kΩ, unless otherwise noted.

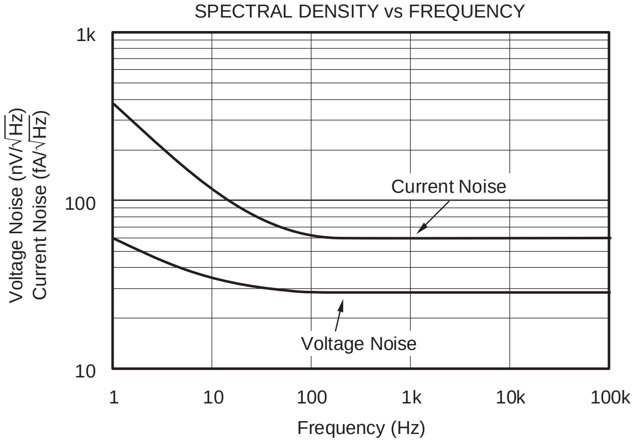
OPEN−LOOP GAIN/PHASE vs FREQUENCY



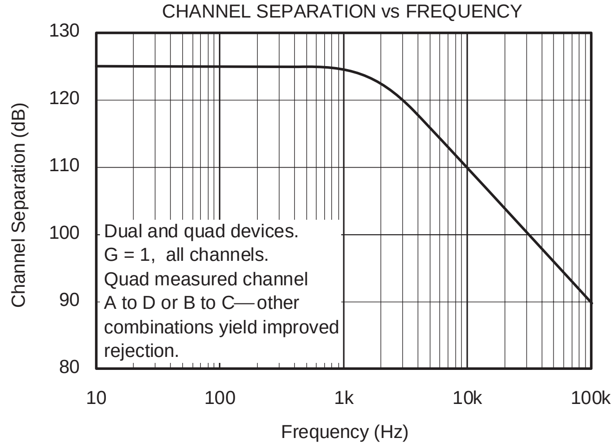
POWER SUPPLY and COMMON−MODE REJECTION
vs FREQUENCY



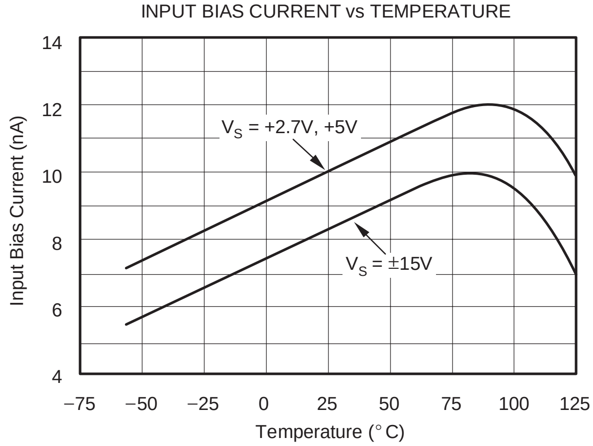
INPUT NOISE AND CURRENT NOISE
SPECTRAL DENSITY vs FREQUENCY



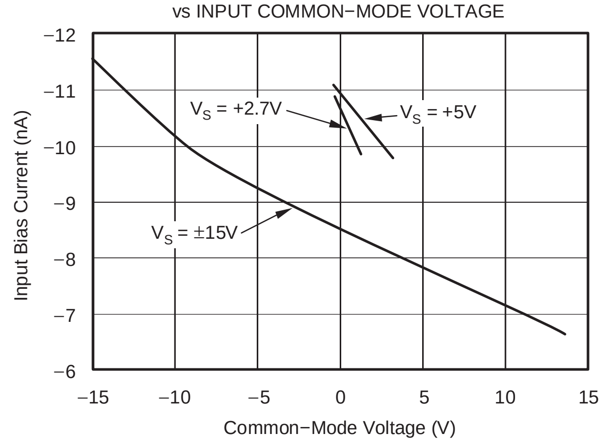
CHANNEL SEPARATION vs FREQUENCY



INPUT BIAS CURRENT vs TEMPERATURE

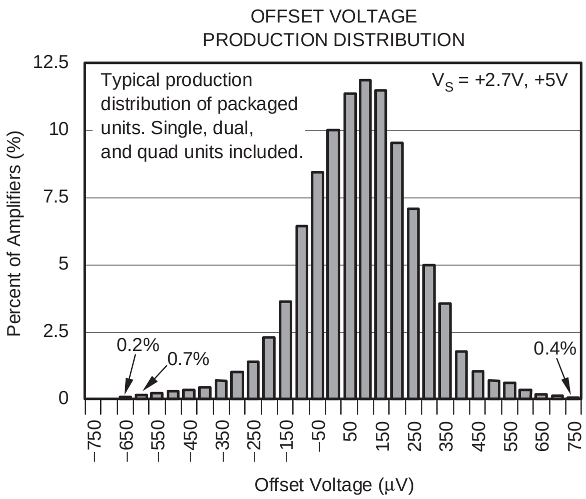


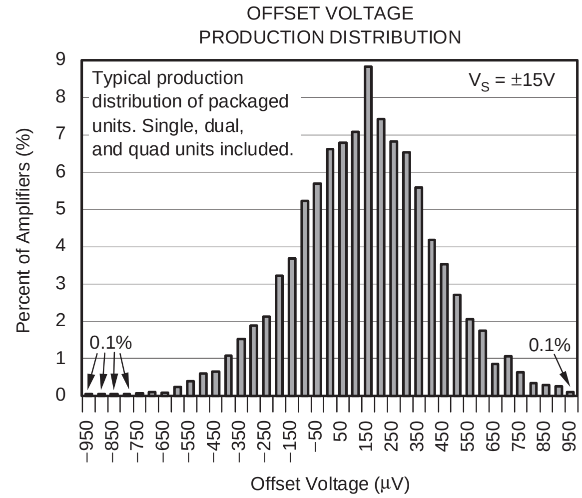
INPUT BIAS CURRENT
vs INPUT COMMON−MODE VOLTAGE

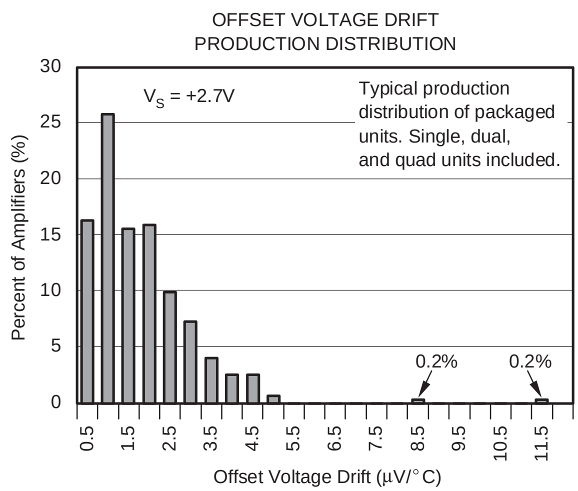


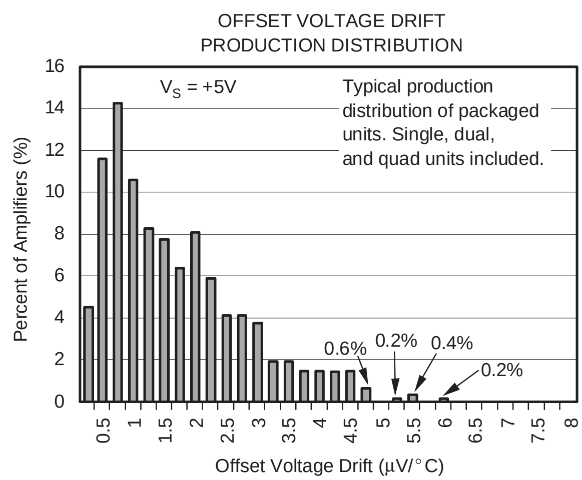
TYPICAL CHARACTERISTICS (Continued)

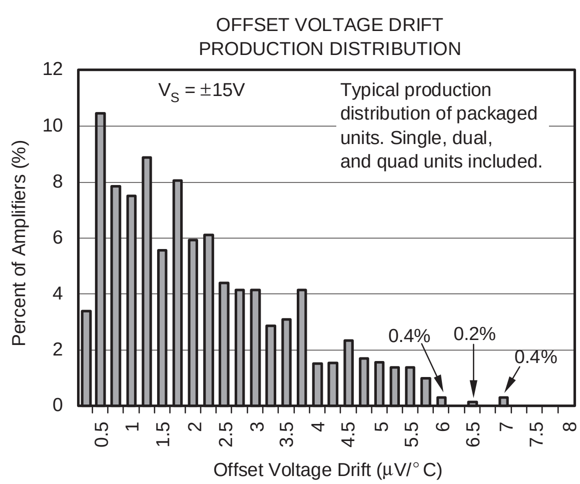
At T_A = +25°C and R_L = 10kΩ, unless otherwise noted.

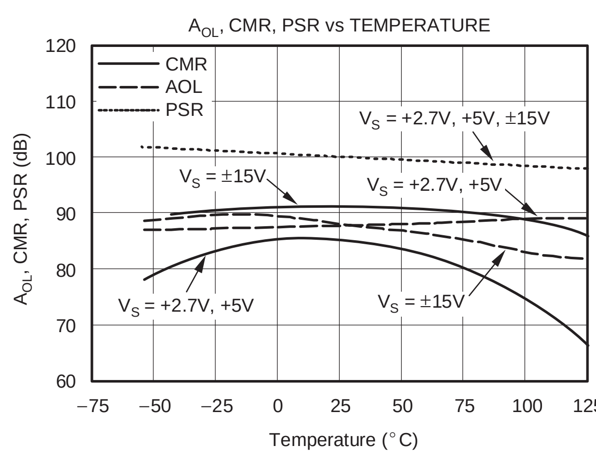








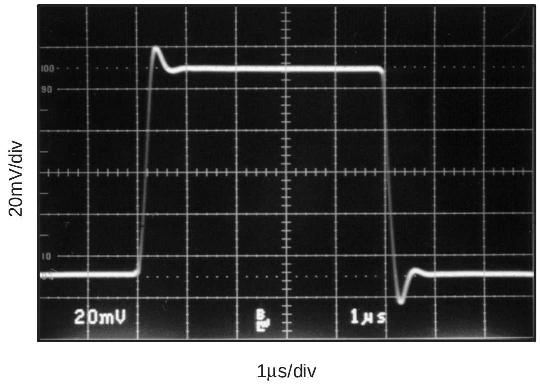




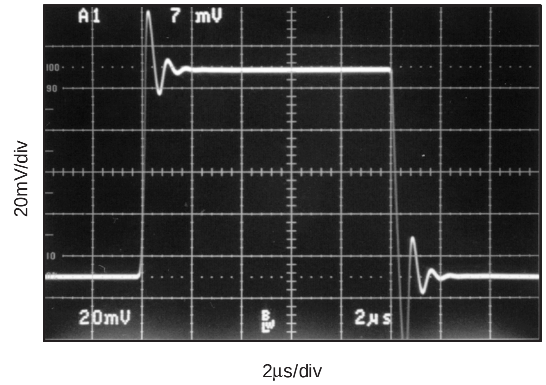
TYPICAL CHARACTERISTICS (Continued)

At T_A = +25°C and R_L = 10kΩ, unless otherwise noted.

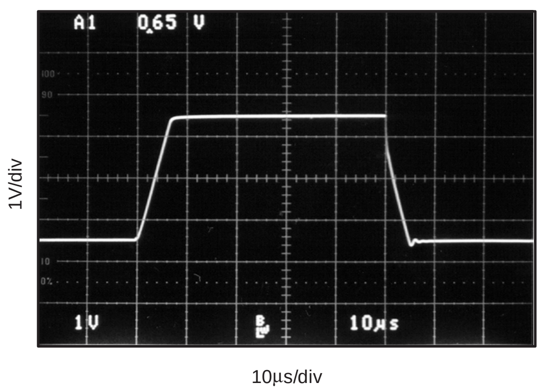
SMALL−SIGNAL STEP RESPONSE
(G = 1, C_L = 100pF, V_S = +5V)



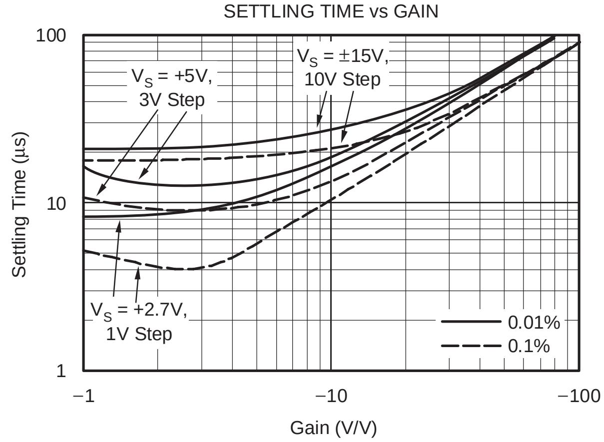
SMALL−SIGNAL STEP RESPONSE
(G = 1, C_L = 220pF, V_S = +5V)



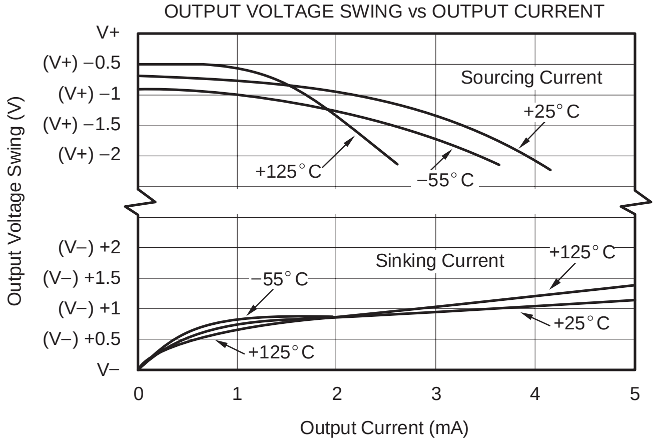
LARGE−SIGNAL STEP RESPONSE
(G = 1, C_L = 100pF, V_S = +5V)



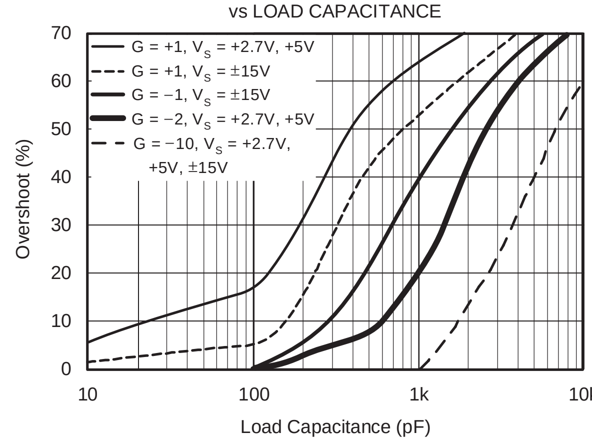
SETTLING TIME vs GAIN



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



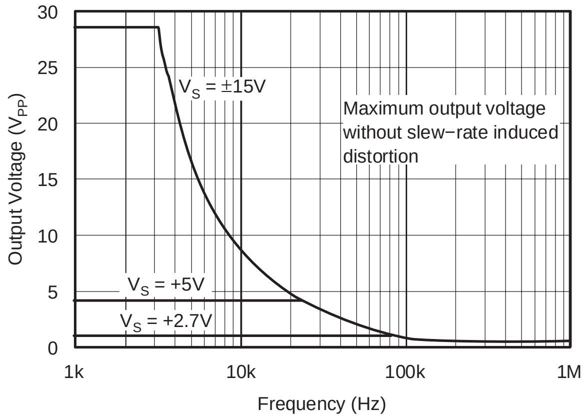
SMALL−SIGNAL OVERSHOOT
vs LOAD CAPACITANCE



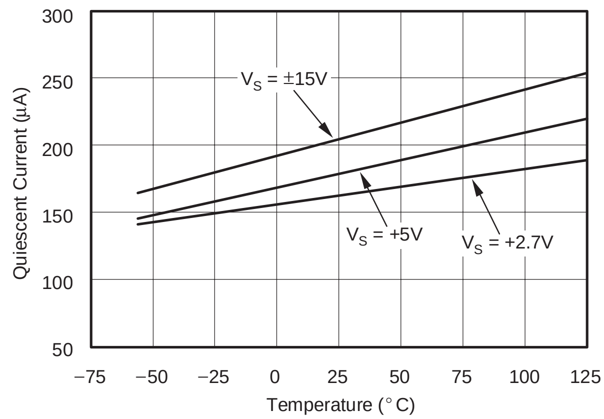
TYPICAL CHARACTERISTICS (Continued)

At T_A = +25°C and R_L = 10kΩ, unless otherwise noted.

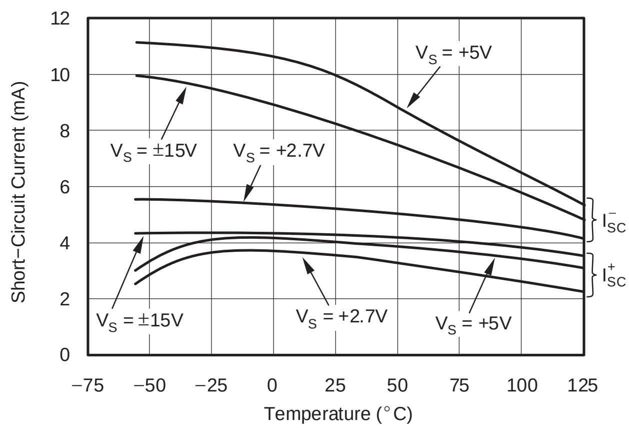
MAXIMUM OUTPUT VOLTAGE
vs FREQUENCY



QUIESCENT CURRENT vs TEMPERATURE



SHORT−CIRCUIT CURRENT vs TEMPERATURE



APPLICATION INFORMATION

OPA237 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power supply pins should be bypassed with 10nF ceramic capacitors.

OPERATING VOLTAGE

OPA237 series op amps operate from single (+2.7V to +36V) or dual (±1.35V to ±18V) supplies with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in typical performance curves. Specifications are production tested with +2.7V, +5V, and ±15V supplies.

OUTPUT CURRENT AND STABILITY

OPA237 series op amps can drive large capacitive loads. However, under certain limited output conditions any op amp may become unstable. Figure 1 shows the region where the OPA237 has a potential for instability. These load conditions are rarely encountered, especially for single supply applications. For example, take the case when a +5V supply with a 10kΩ load to $V_S/2$ is used. OPA237 series op amps remain stable with capacitive loads up to 4,000pF, if sinking current and up to 10,000pF, if sourcing current. Furthermore, in single-supply applications where the load is connected to ground, the op amp is only sourcing current, and as shown Figure 1, can drive 10,000pF with output currents up to 1.5mA.

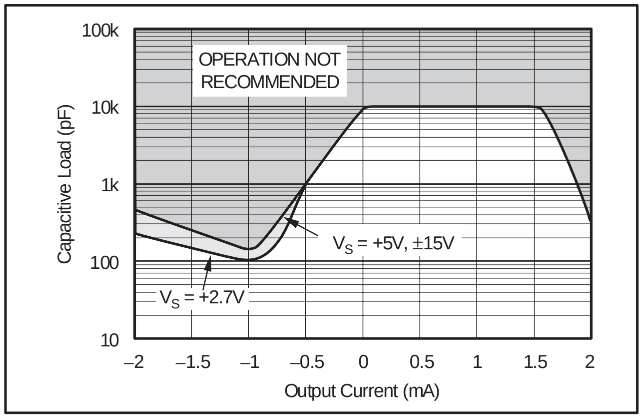


Figure 1. Stability-Capacitive Load vs Output Current

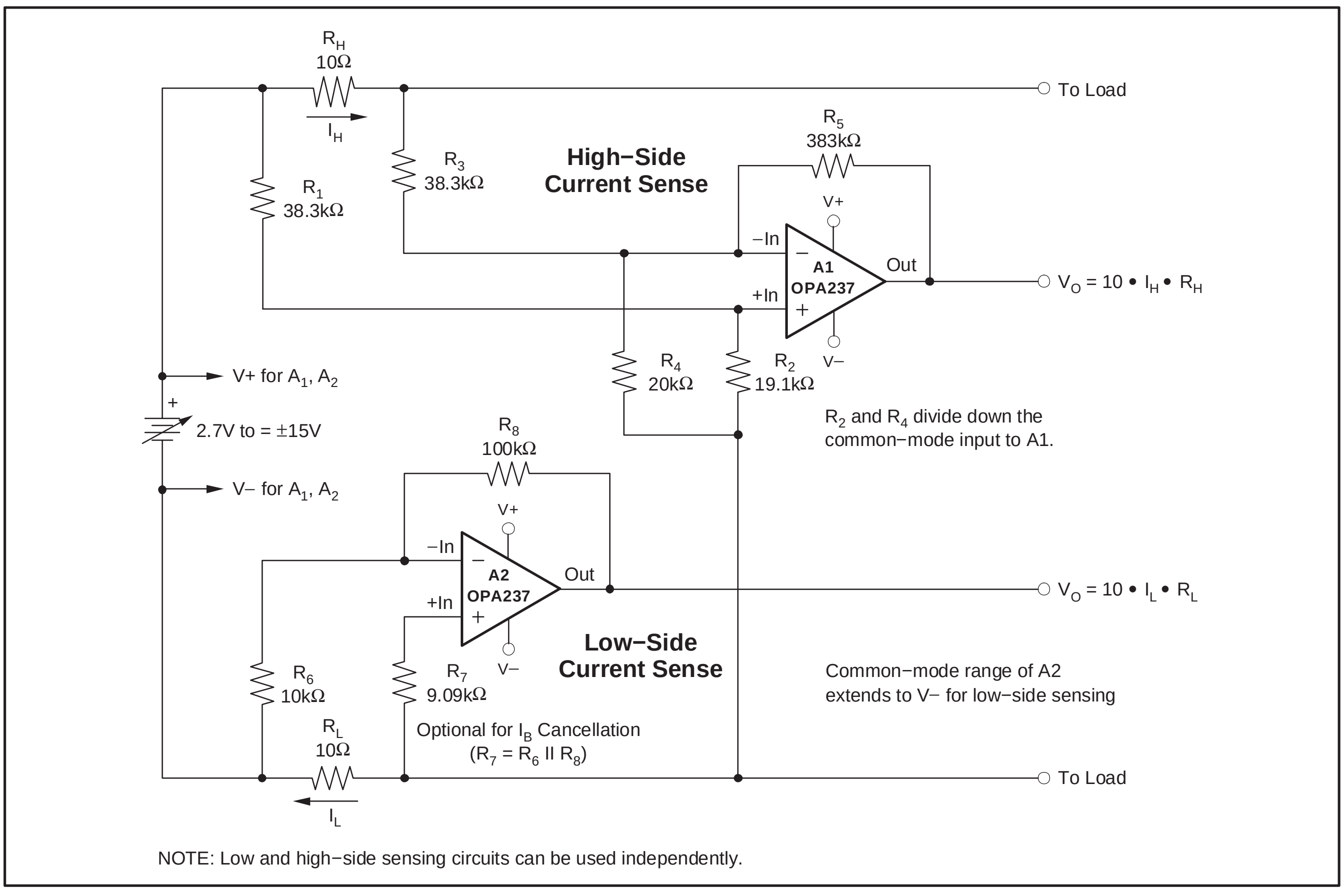


Figure 2. Low and High-Side Battery Current Sensing

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2237EA/250	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR		B37A	Samples
OPA2237EA/2K5	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	B37A	Samples
OPA2237UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR		OPA 2237UA	Samples
OPA2237UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR		OPA 2237UA	Samples
OPA2237UAE4	ACTIVE	SOIC	D	8	75	TBD	Call TI	Call TI			Samples
OPA237NA/250	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 70	A37A	Samples
OPA237NA/250E4	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 70	A37A	
OPA237NA/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 70	A37A	Samples
OPA237NA/3KE4	LIFEBUY	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 70	A37A	
OPA237UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 70	OPA 237UA	Samples
OPA237UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 70	OPA 237UA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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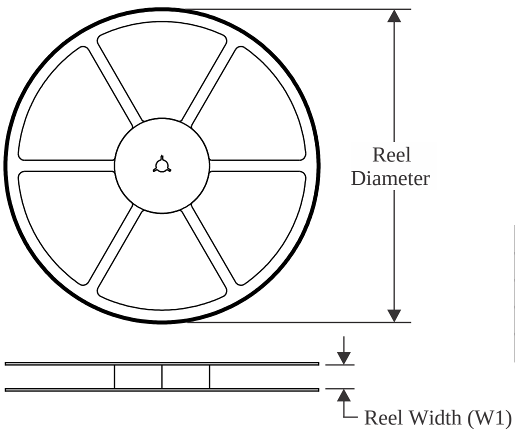
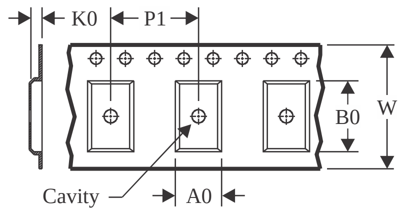
TAPE AND REEL INFORMATION

REEL DIMENSIONS

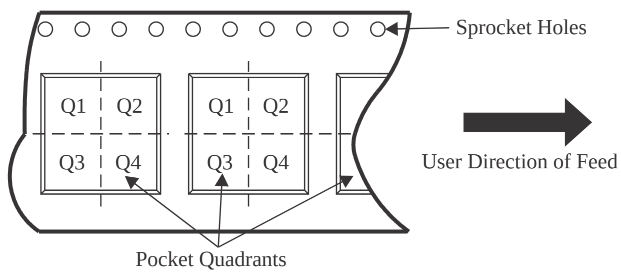


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

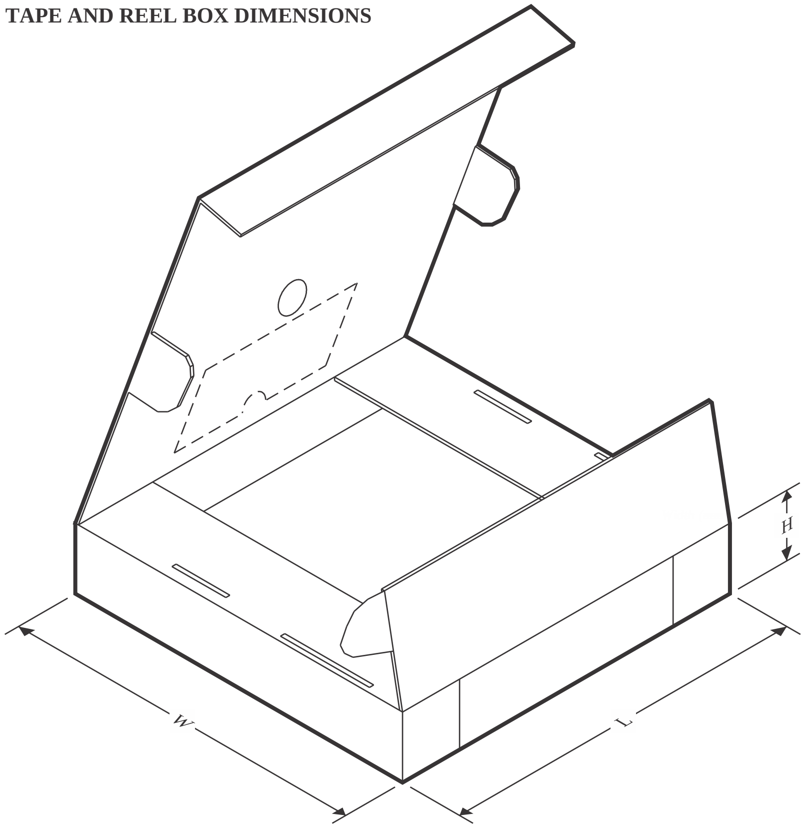
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2237EA/250	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2237EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2237UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA237NA/250	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA237NA/3K	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA237UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

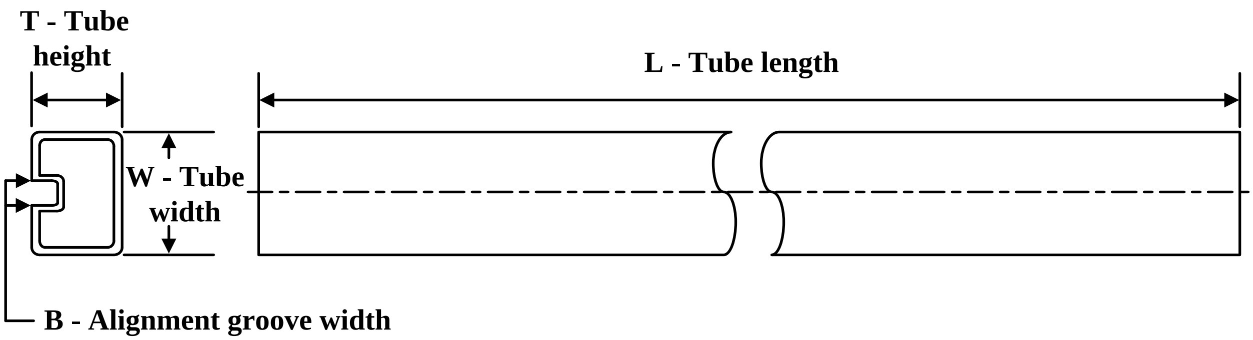
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

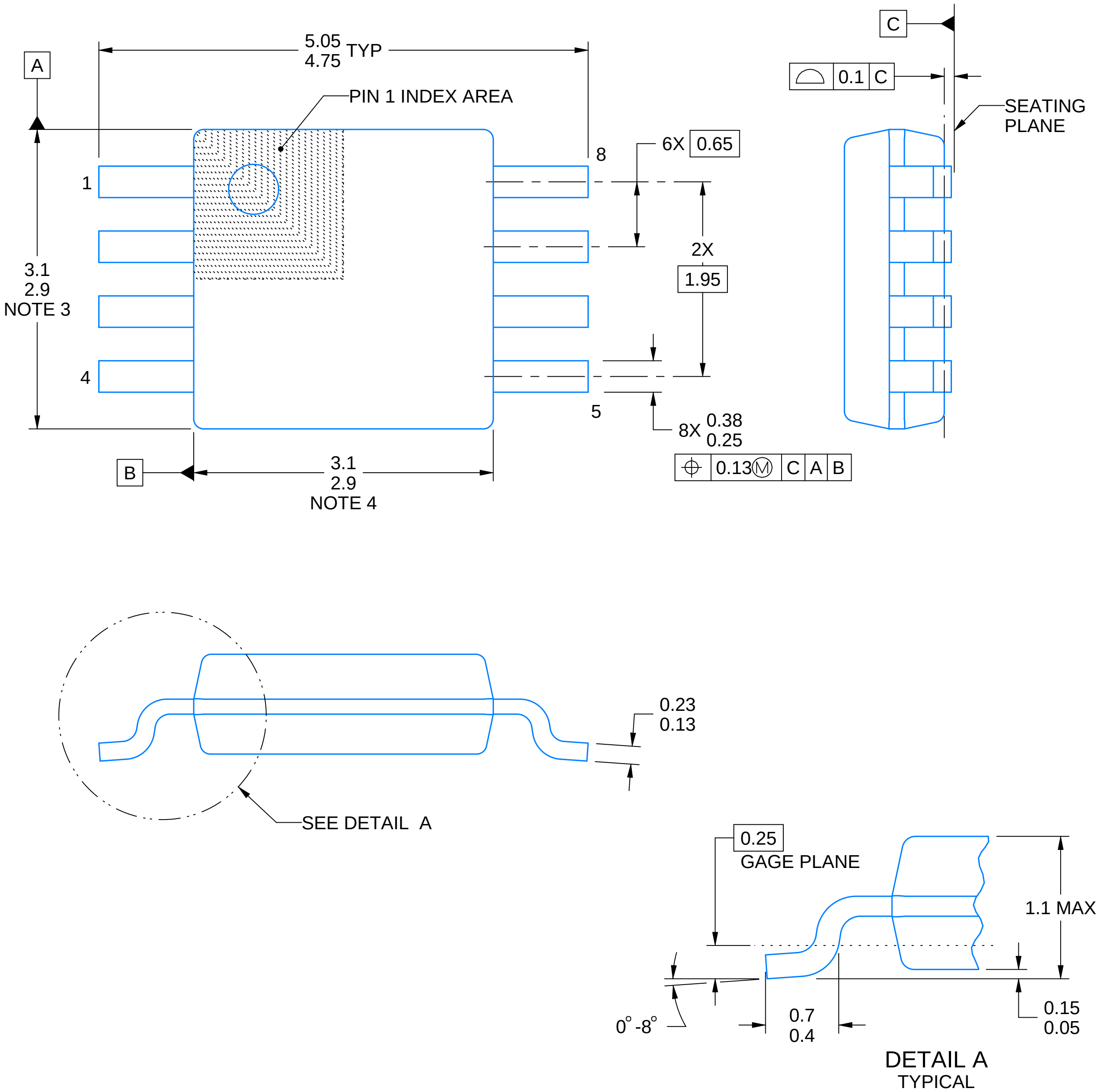
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2237EA/250	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2237EA/2K5	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2237UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA237NA/250	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA237NA/3K	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA237UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2237UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA237UA	D	SOIC	8	75	506.6	8	3940	4.32

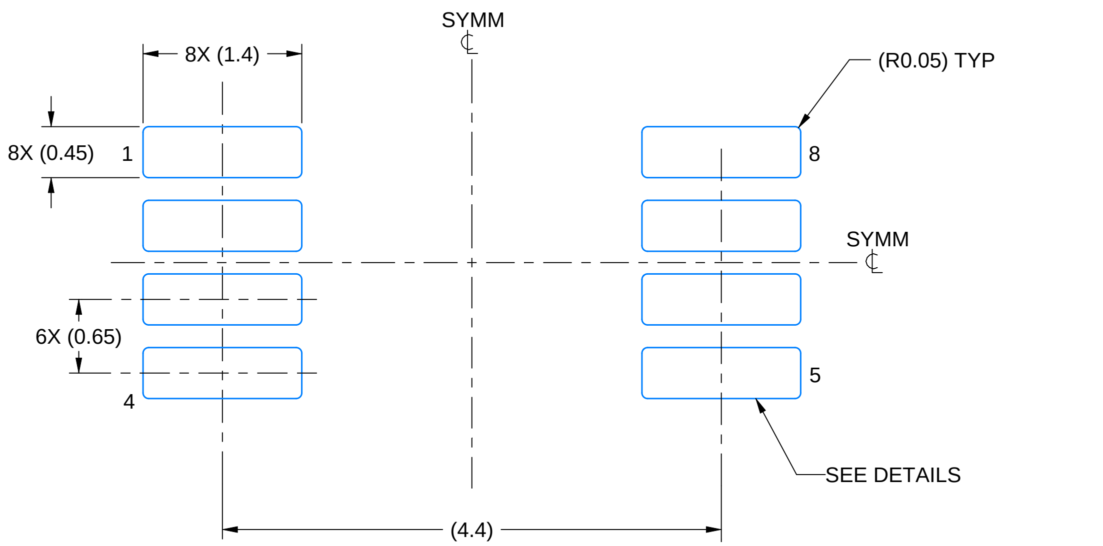


4214862/A 04/2023

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



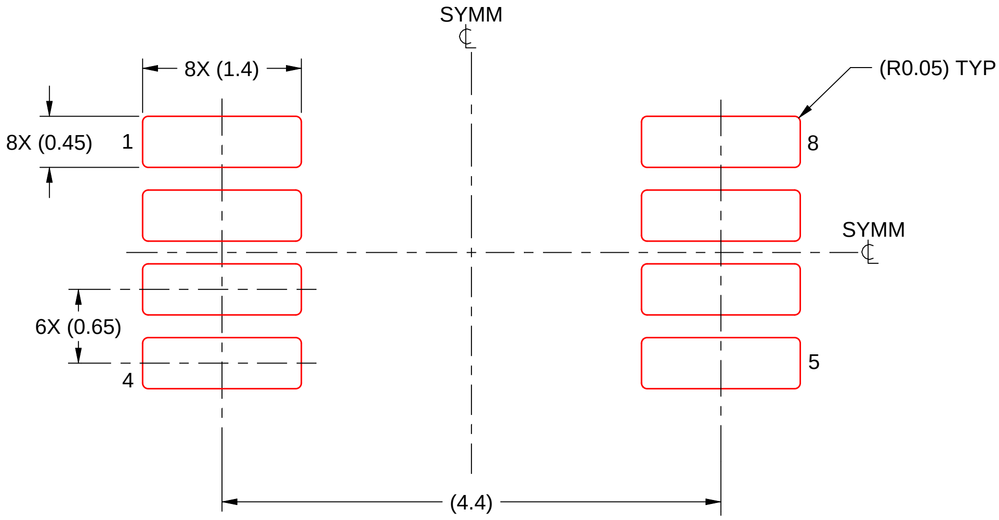
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

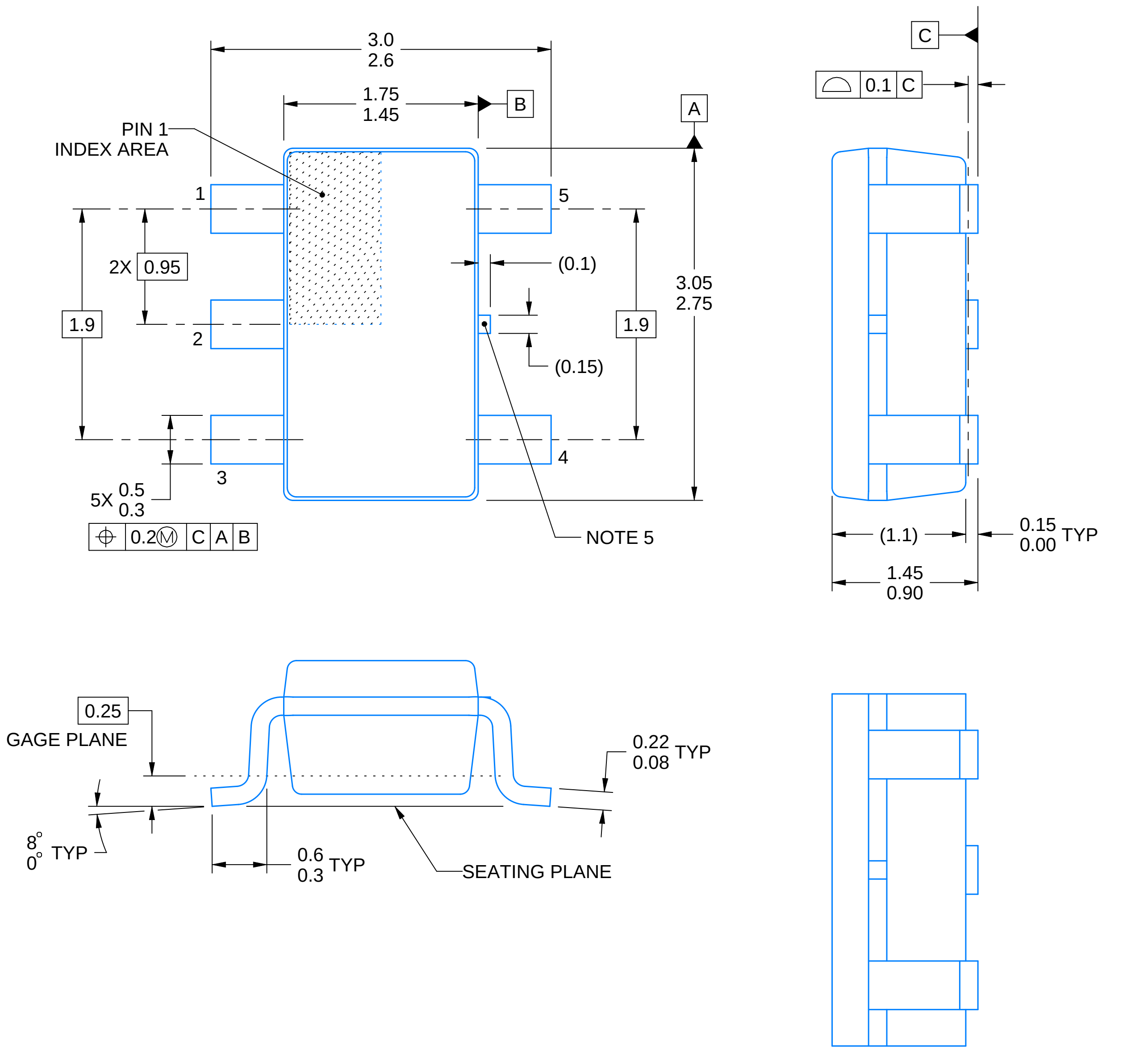


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

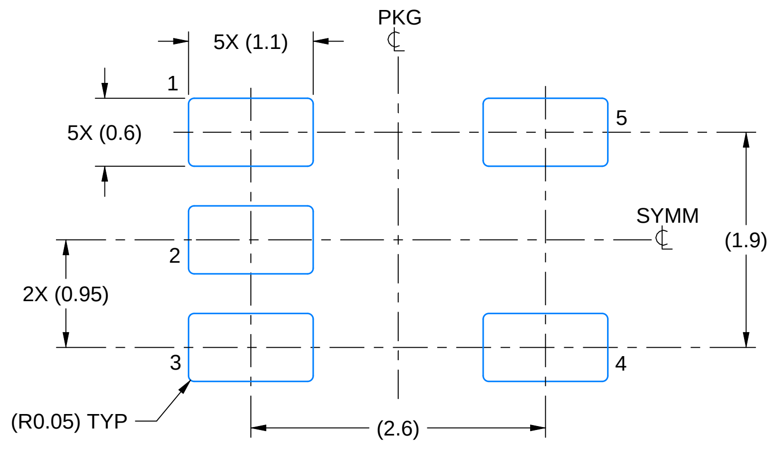


ALTERNATIVE PACKAGE SINGULATION VIEW

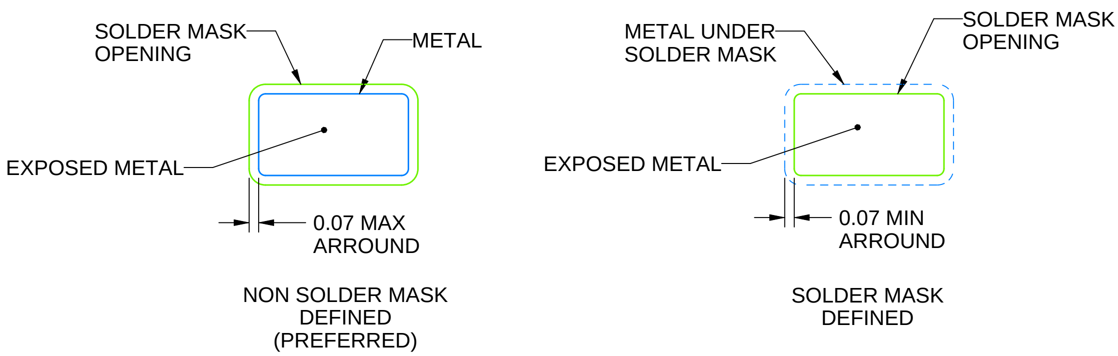
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

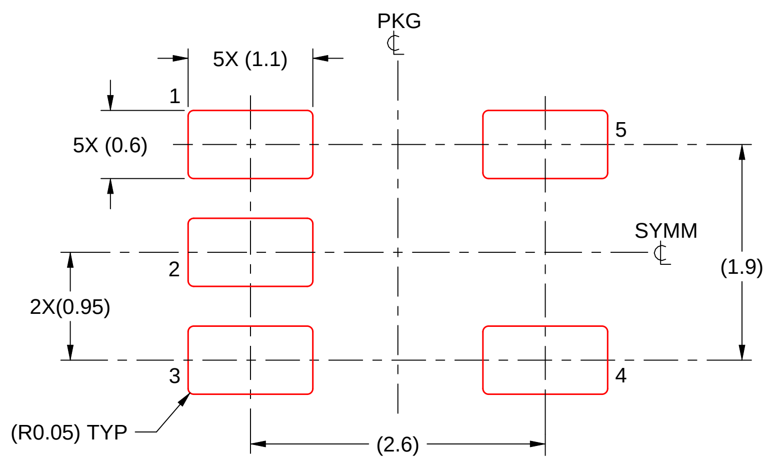


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

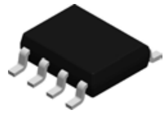


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

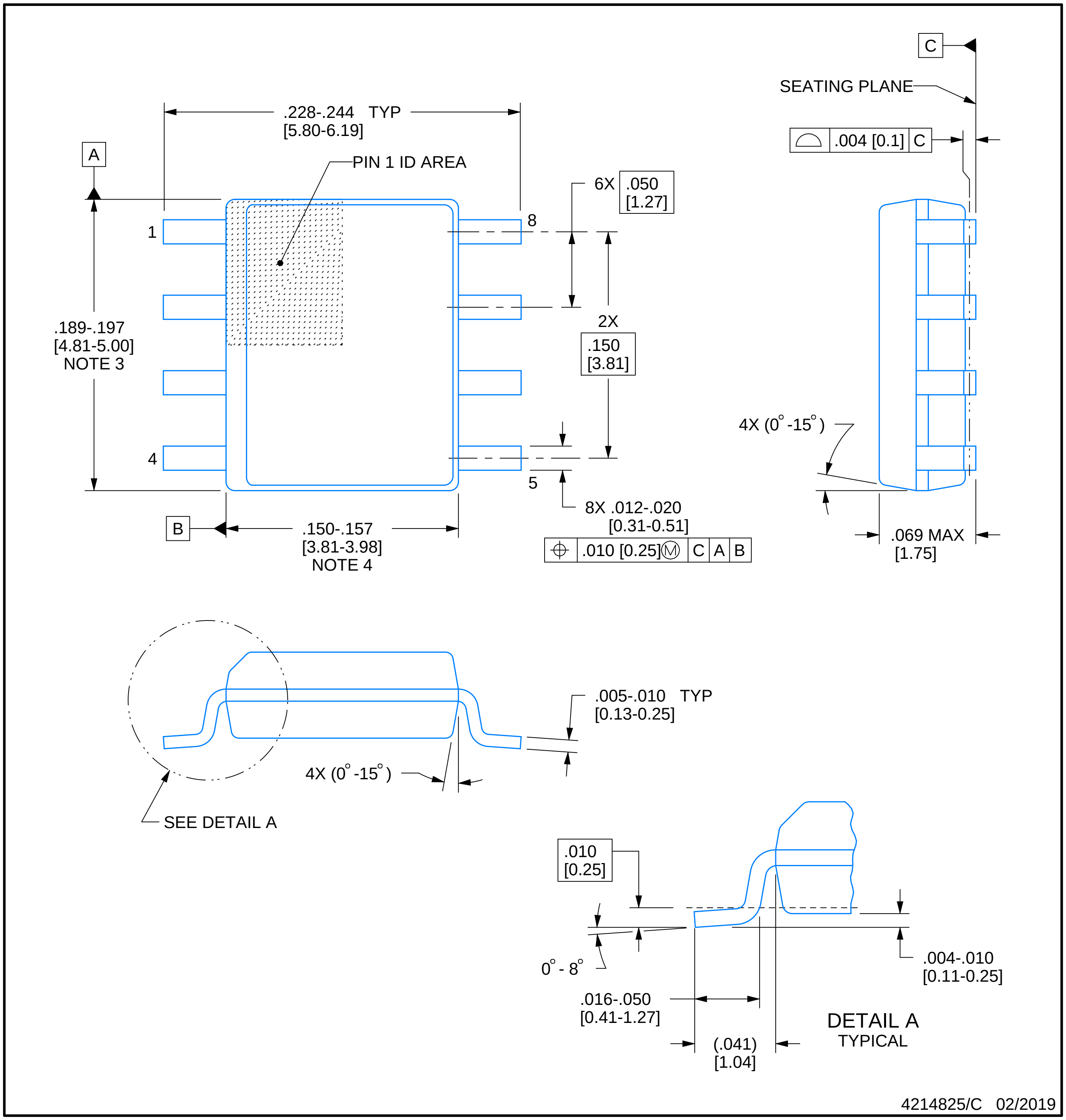
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D0008A

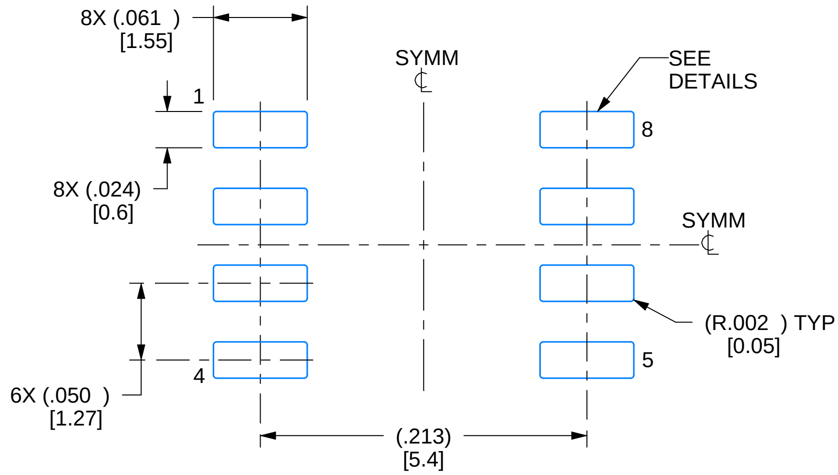
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

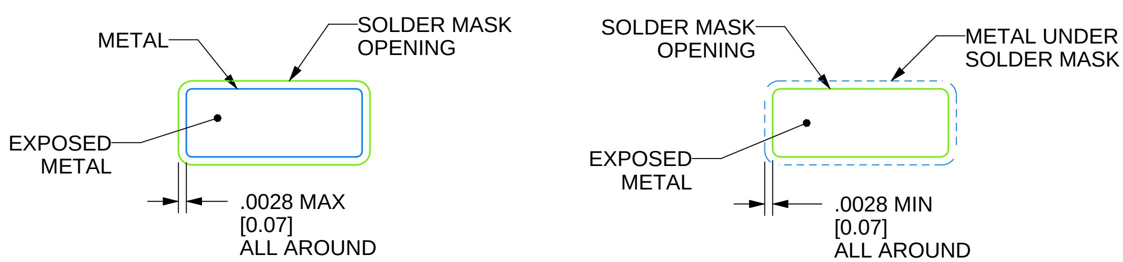


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

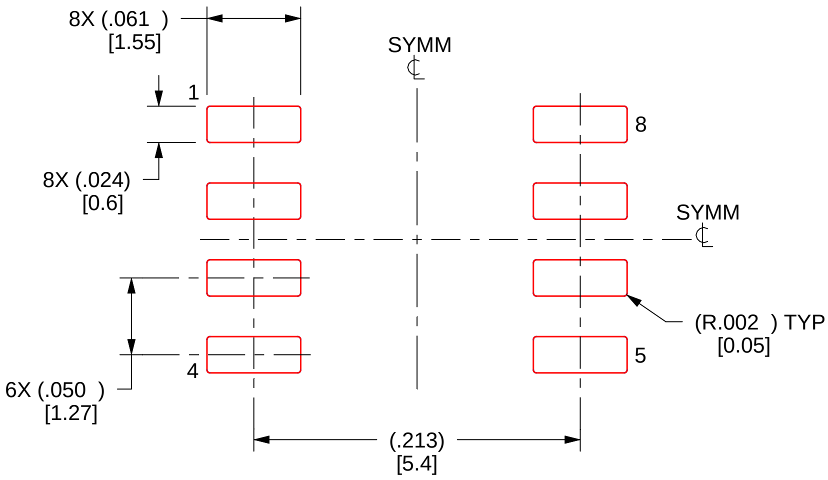
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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