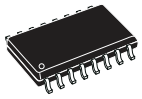
L4976

1 A step-down switching regulator

Datasheet - production data



SO16W

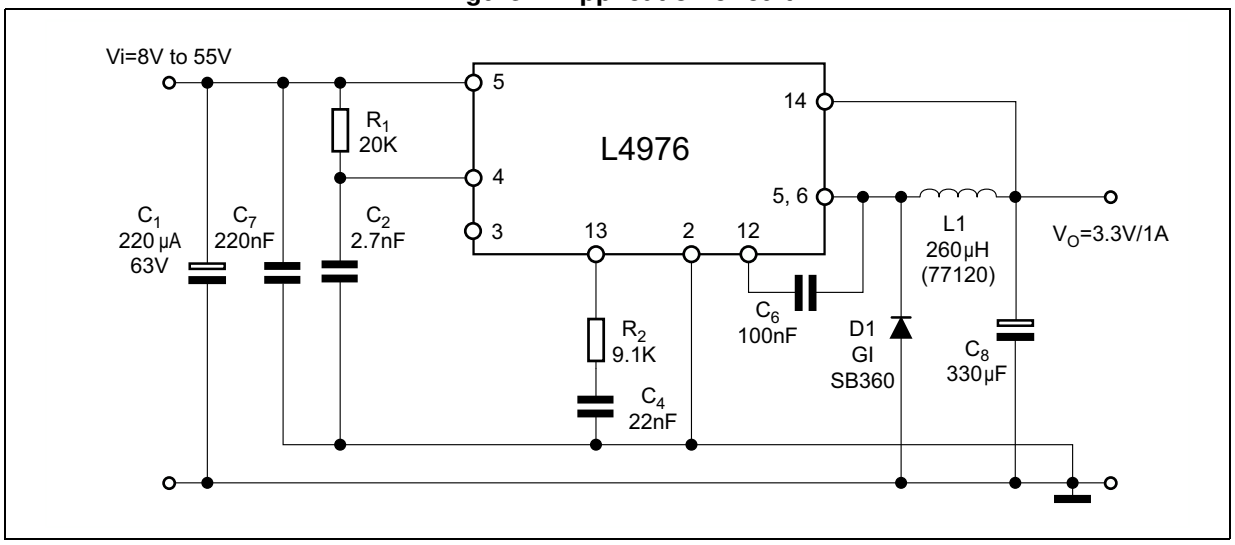
Features

- Up to 1 A step-down converter
- Operating input voltage from 8 V to 55 V
- Precise 5.1 V reference voltage
- Output voltage adjustable from 0.5 V to 50 V
- Switching frequency adjustable up to 300 kHz
- Voltage feed-forward
- Zero load current operation
- Internal current limiting (pulse-by-pulse and hiccup mode)
- Protection against feedback disconnection
- Thermal shutdown

Description

The L4976 is a step-down monolithic power switching regulator delivering 1 A at a voltage between 3.3 V and 50 V (selected by a simple external divider). Realized in BCD mixed technology, the device uses an internal power D-MOS transistor (with a typical $R_{ds(ON)}$ of 0.25 Ω) to obtain very high efficency and high switching speed. A switching frequency up to 300 kHz is achievable (the maximum power dissipation of the packages must be observed). A wide input voltage range between 8 V to 55 V and output voltages regulated from 3.3 V to 40 V cover the majority of today's applications. Features of this new generations of DC-DC converter include pulse-by-pulse current limit, hiccup mode for short circuit protection, voltage feedforward regulation, protection against feedback loop disconnection and thermal shutdown. The device is available in plastic dual in line, SO16W for SMD assembly.

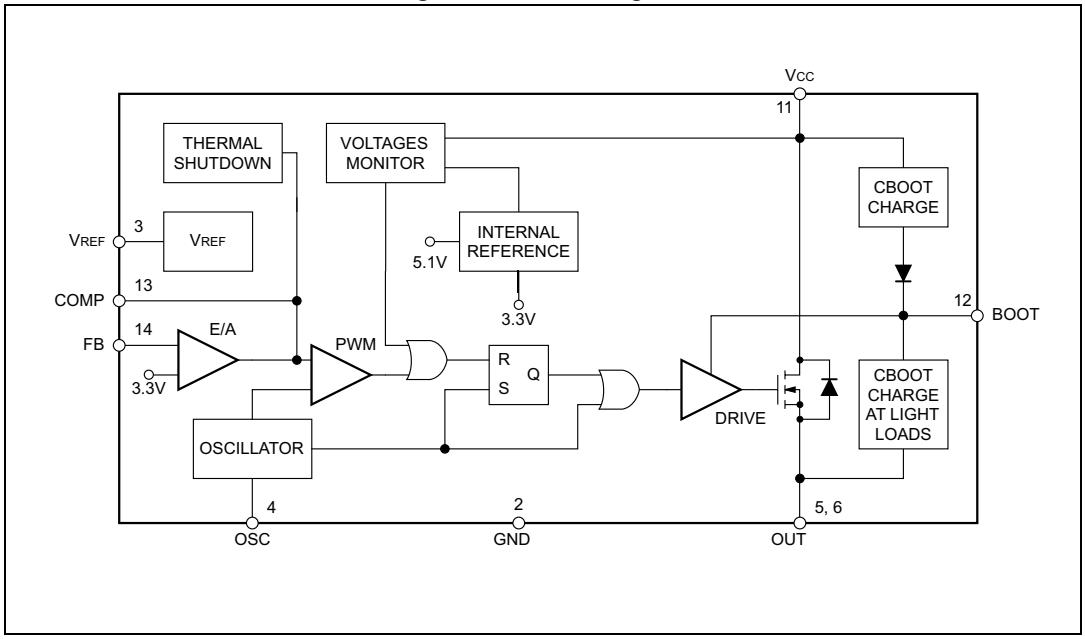
Figure 1. Application circuit



Contents

1 Block diagram

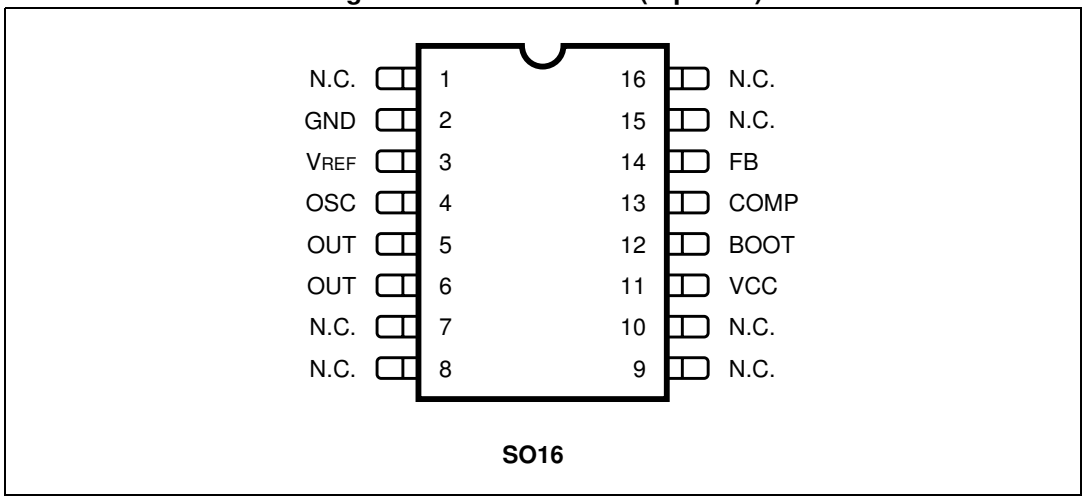
Figure 2. Block diagram



2 Pin settings

2.1 Pin connection

Figure 3. Pin connection (top view)



2.2 Pin description

Table 1. Pin description

N° Pin (1)	Name	Description
2	GND	Ground
3	VREF	5.1 V Reference voltage with 20 mA current capability.
4	OSC	An external resistor connected between the unregulated input voltage and this pin and a capacitor connected from this pin to ground fix the switching frequency. (Line feed forward is automatically obtained)
5, 6	OUT	Stepdown regulator output.
11	VCC	Unregulated DC input voltage.
12	BOOT	A capacitor connected between this pin and OUT allows to drive the internal VDMOS.
13	COMP	E/A output to be used for frequency compensation.
14	FB	Stepdown feedback input. Connecting directly to this pin results in an output voltage of 3.3 V. An external resistive divider is required for higher output voltages.

1. Pins 1, 7, 8, 9, 10, 15 and 16 are not internally, electrically connected to the die.

3 Electrical data

3.1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V11	Input voltage		58	V
V5, V6	Output DC voltage		-1	V
	Output peak voltage at t = 0.1 µs, f = 200 kHz		-5	V
I5, I6	Maximum output current		internal limit	
V12-V11			14	V
V12	Bootstrap voltage		70	V
V13	Analogs input voltage (V_{CC} = 24 V)		12	V
V14	(V_{CC} = 20 V)		6	V
			-0.3	V
P_{TOT}	Power dissipation a $T_A \leq 60°C$	SO16	0.8	W
T_J, T_{STG}	Junction and storage temperature		-40 to 150	°C

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	S016W	Unit
R_{thJA}	Maximum thermal resistance junction-ambient	110 (1)	°C/W

1. Package mounted on board

3.3 Operating temperature rating

Table 4. Operating temperature rating

Symbol	Parameter	Value	Unit
T_J	Junction temperature range	-40 to 150	°C

4 Electrical characteristics

Table 5. Electrical characteristics
(T_J = 25°C, C_{OSC} = 2.7nF, R_{OSC} = 20kΩ, V_{CC} = 24V, unless otherwise specified.)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Dynamic characteristic						
V_I	Operating input voltage range	V_O = 3.3 to 50V; I_O = 1A (1)	8		55	V
V_O	Output voltage	I_O = 0.5A	3.33	3.36	3.39	V
		I_O = 0.2 to 1A	3.292	3.36	3.427	V
		V_{CC} = 8 to 55V (1)	3.22	3.36	3.5	V
Vd	Dropout voltage	V_{CC} = 10V; I_O = 1A		0.29	0.367	V
		(1)			0.587	V
I_l	Maximum limiting current	V_{CC} = 8 to 55V (1)	1.5	2	2.5	A
	Efficiency	V_O = 3.3V; I_O = 1A		85		%
f_s	Switching frequency	(1)	90	100	110	kHz
SVRR	Supply voltage ripple rejection	$V_I = V_{CC} + 2V_{RMS}$; $V_O = V_{ref}$; I_O = 1.A; f_{ripple} = 100Hz	60			dB
	Voltage stability of switching frequency	V_{CC} = 8 to 55V		3	6	%
	Temp. stability of switching frequency	T_J = 0 to 125°C		4		%
Reference section						
	Reference voltage		5.0	5.1	5.2	V
		I_{ref} = 0 to 10mA; (1)	4.950	5.1	5.250	V
		V_{CC} = 8 to 55V				
	Line regulation	I_{ref} = 0mA;		5	10	mV
		V_{CC} = 8 to 55V				
	Load regulation	V_{ref} = 0 to 5mA;		2	10	mV
		V_{CC} = 0 to 20mA		6	25	mV
	Short circuit current		30	65	100	mA

Table 5. Electrical characteristics (continued)
(T_J = 25°C, C_{OSC} = 2.7nF, R_{OSC} = 20kΩ, V_{CC} = 24V, unless otherwise specified.)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
DC Characteristics						
I_{qop}	Total operating quiescent current			4	6	mA
I_q	Quiescent current	Duty Cycle = 0; V_{FB} = 3.8V		2.5	3.5	mA
Error Amplifier						
V_{FB}	Voltage feedback input		3.33	3.36	3.39	V
R_L	Line regulation	V_{CC} = 8 to 55V		5	10	mV
	Ref. voltage stability vs temperature	(1)		0.4		mV/°C
V_{oH}	High level output voltage	V_{FB} = 2.5V	10.3			V
V_{oL}	Low level output voltage	V_{FB} = 3.8V			0.65	V
$I_{O\ source}$	Source output current	V_{comp} = 6V; V_{FB} = 2.5V	180	220		µA
$I_{O\ sink}$	Sink output current	V_{comp} = 6V; V_{FB} = 3.8V	200	300		µA
I_b	Source bias current			2	3	µA
SVRR E/A	Supply voltage ripple rejection	V_{comp} = Vfb; V_{CC} = 8 to 55V	60	80		dB
	DC open loop gain	R_L = ∞	50	57		dB
gm	Transconductance	I_{comp} = -0.1 to 0.1mA V_{comp} = 6V		2.5		ms
Oscillator section						
	Ramp valley		0.78	0.85	0.92	V
	Ramp peak	V_{CC} = 8V	2	2.15	2.3	V
		V_{CC} = 55V	9	9.6	10.2	V
	Maximum duty cycle		95	97		%
	Maximum frequency	Duty cycle = 0% R_{osc} = 13kW, C_{osc} = 820pF			300	kHz

1. Specification refered to Tj from 0 to 125°C

5 Typical charcteristics

Figure 4. Quiescent drain current vs. input voltage

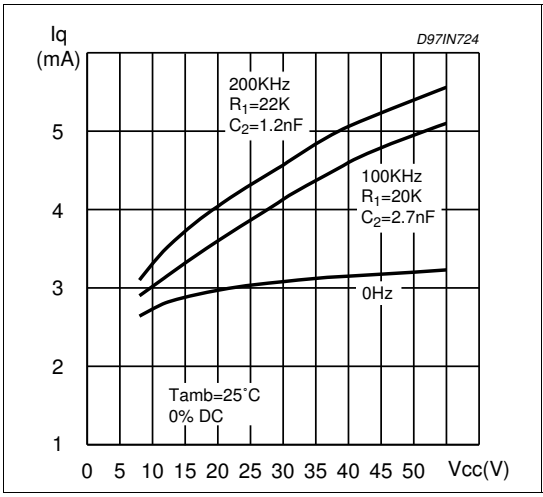


Figure 5. Line regulation

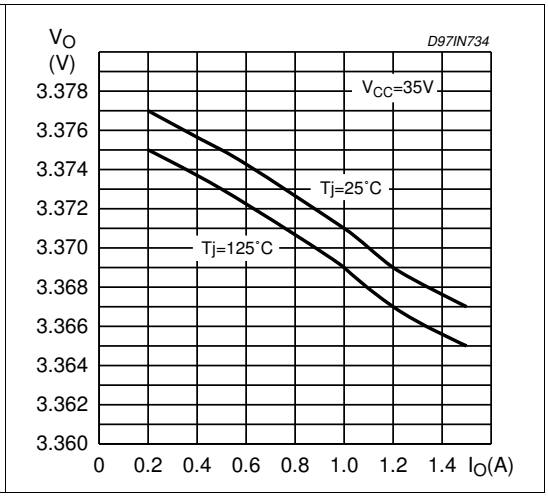


Figure 6. Quiescent current vs. junction temperature

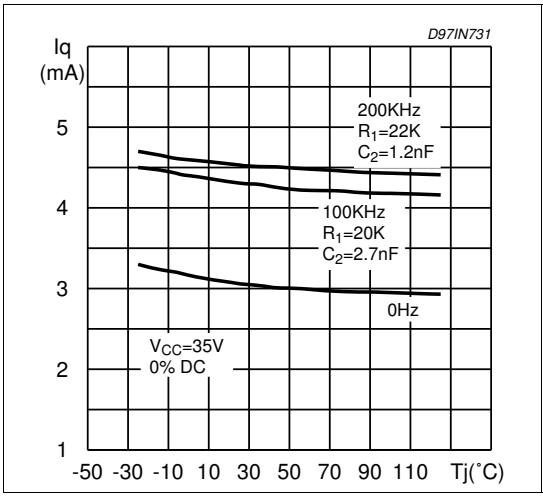


Figure 7. Switching frquency vs. R1 and C2

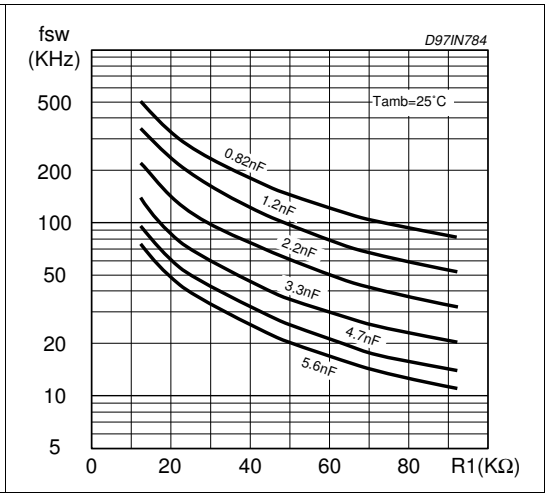


Figure 8. Load regulation

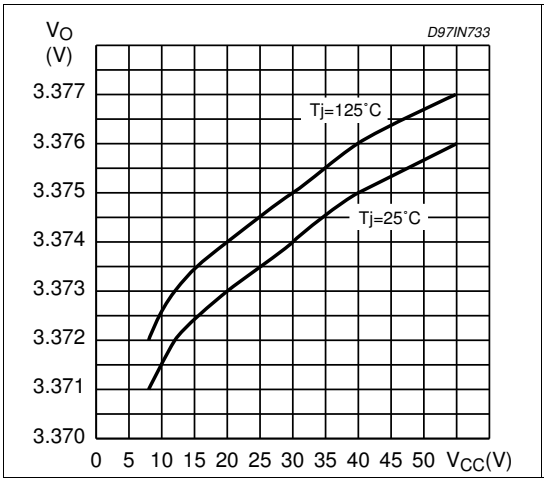


Figure 9. Switching frequency vs. input voltage

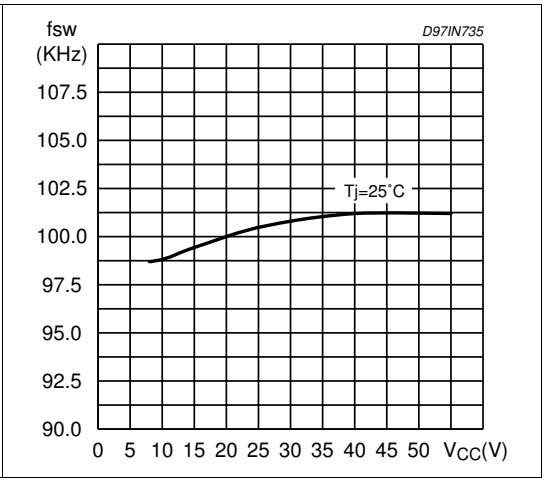


Figure 10. Switching frequency vs. junction temperature

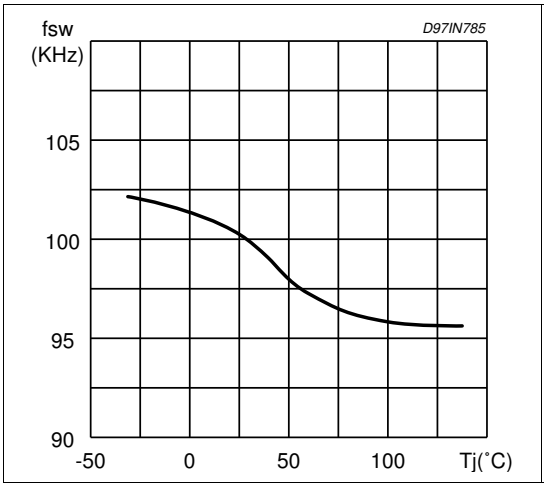


Figure 11. Efficiency vs. output current

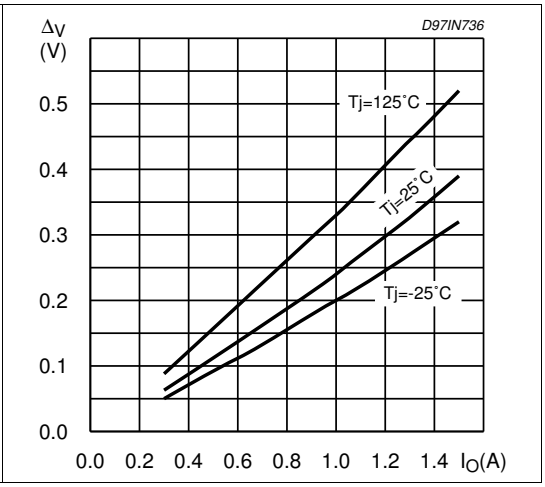


Figure 12. Dropout voltage between pin 5 and 4

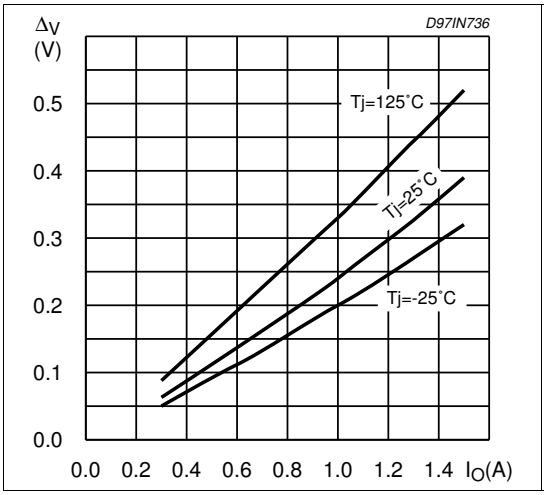


Figure 13. Efficiency vs. output current

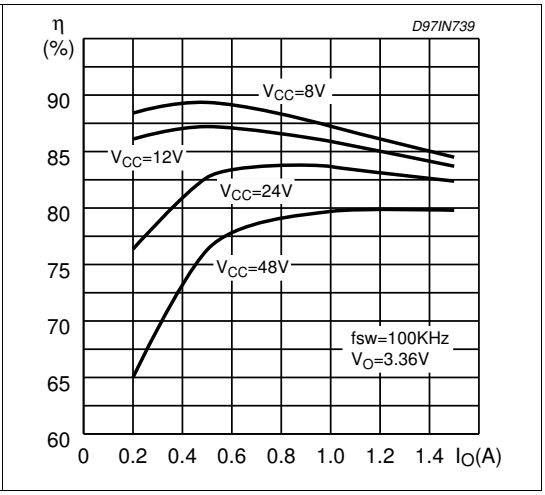


Figure 14. Efficiency vs output voltage

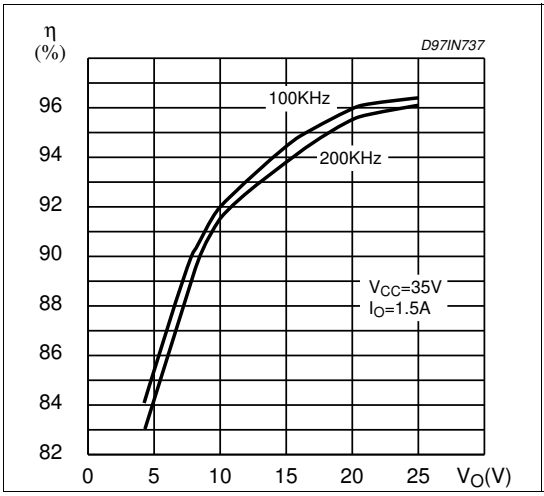


Figure 15. Efficiency vs. output current

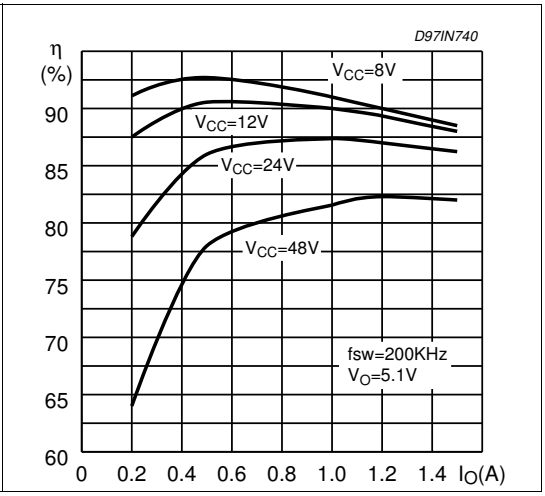


Figure 16. Efficiency vs. output current

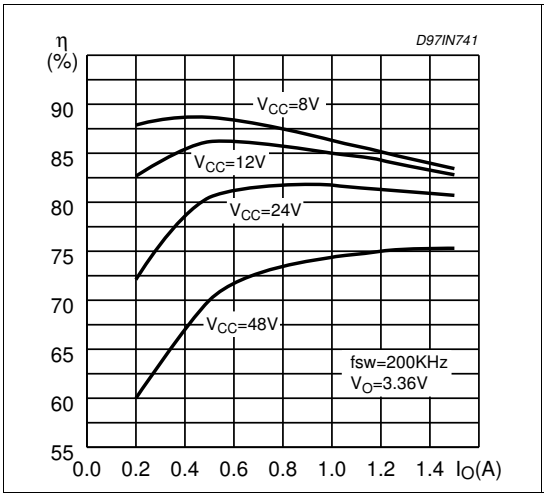


Figure 17. Efficiency vs. Vo

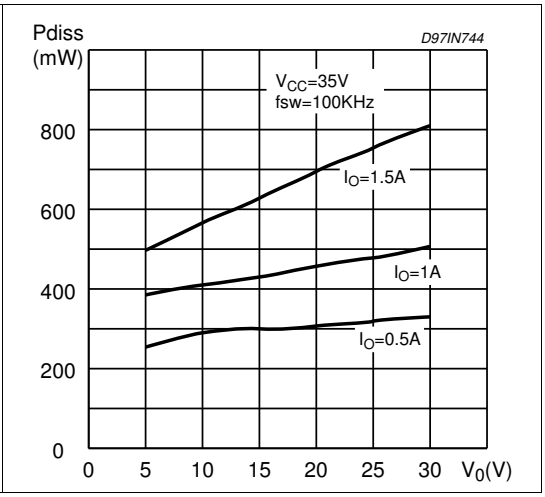


Figure 18. Efficiency vs. V_{CC}

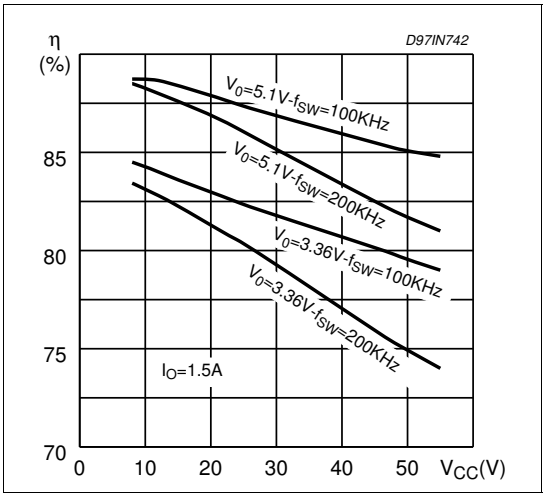


Figure 19. Pulse by pulse limiting current vs. junction temperature.

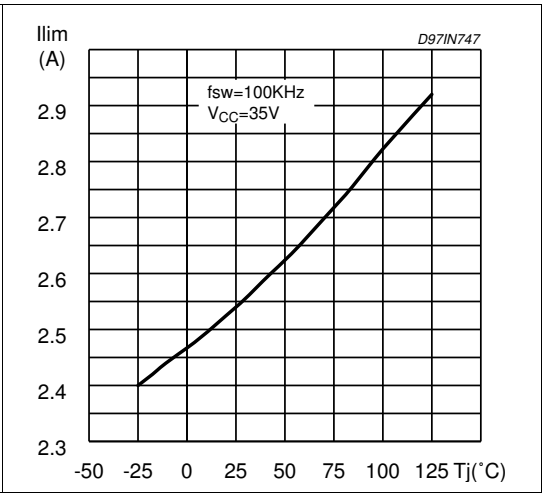


Figure 20. Power dissipation vs. V_{CC}

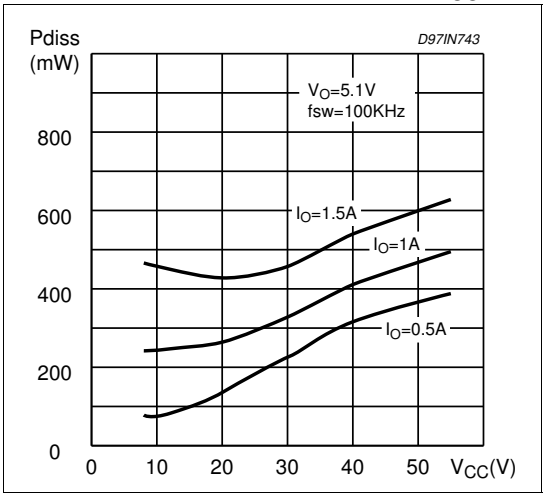


Figure 21. Load transient

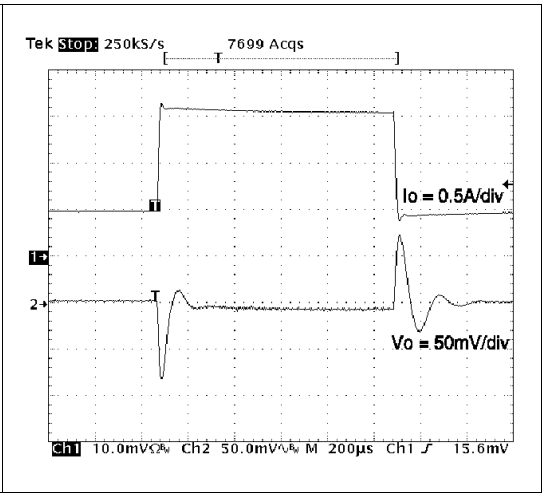


Figure 22. Line transient

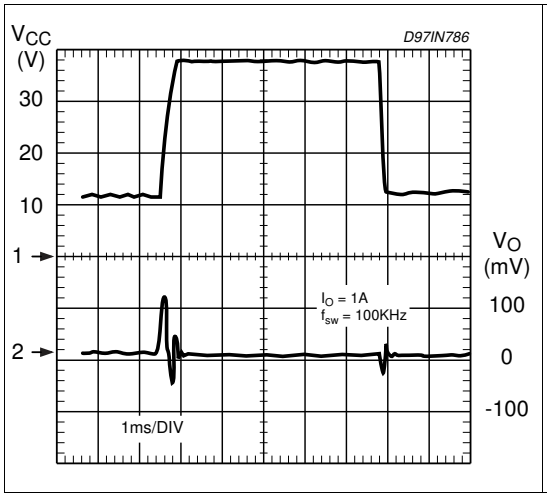
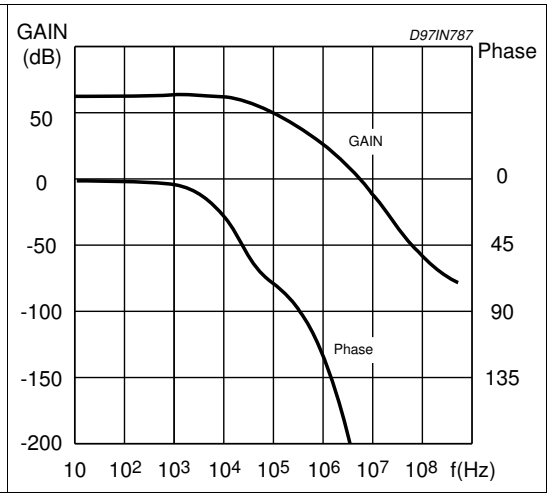


Figure 23. Open loop frequency and phase of error amplifier



6 Package mechanical data

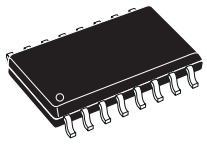
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 24. SO16Wide mechanical data & package dimensions

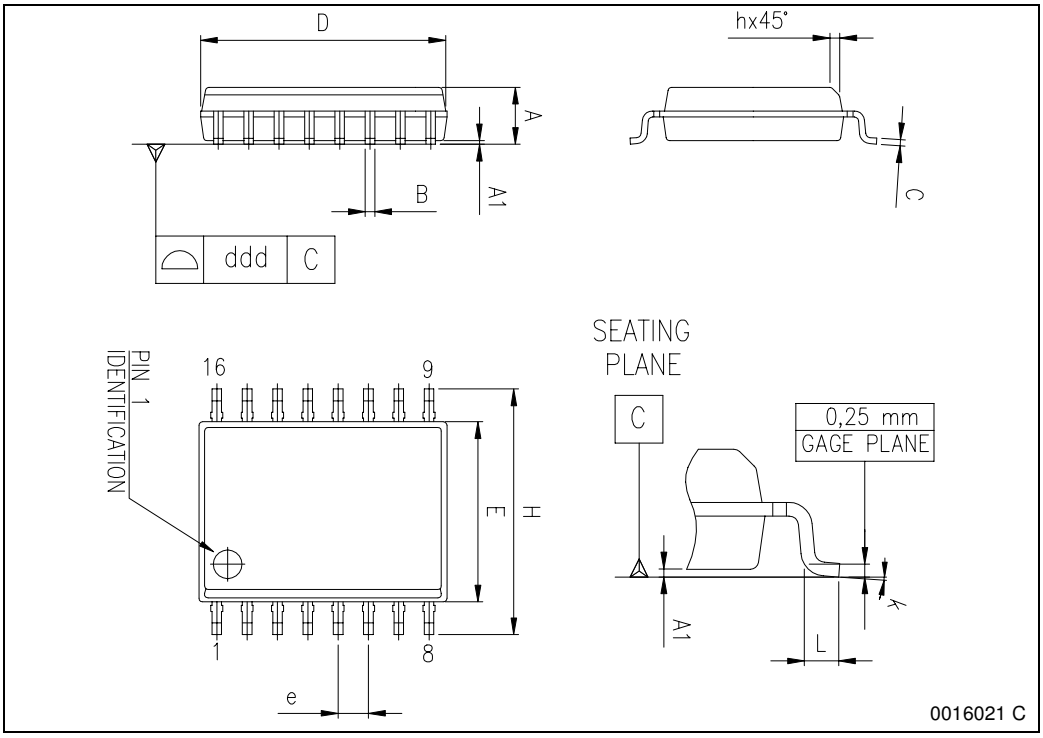
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	10.10		10.50	0.398		0.413
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



SO16 (Wide)



7 Order code

Table 6. Order code

Part number	Package	Packaging
L4976D013TR	SO16W	Tape and reel

8 Revision history

Table 7. Revision history

Date	Revision	Changes
5-Aug-2001	6	First Issue
3-Apr-2007	7	Document reformatted, updated dropout voltage values in Table 5 on page 6
14-May-2024	8	Updated *Table 6*